µc-Si SOLAR CELLS BY DIRECT DEPOSITION WITH APCVD

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ABSTRACT: The rapid thermal direct deposition of micro-crystalline silicon (µc-Si) layers by atmospheric pressure chemical vapour deposition (APCVD) can be done on different intermediate layers and on various substrates. The deposition is done at temperatures between 850 °C and 950 °C is also possible on glass substrates like borosilicate glass [3] or in general substrates with a low critical exposure temperature. In Fig.1 the two concepts for µc-Si solar cells presented in this paper are shown. The major difference between the concepts is the contact formation. In the case of the single side contact formation (see Fig. 1 bottom) the substrates do not have to be conductive. However, in both concepts the µc-Si layers are directly grown on substrates with SiOx as intermediate layer. Furthermore three different emitters, a µc-Si epitaxial emitter, an emitter by POCl3 diffusion and an amorphous silicon (a-Si) heteroemitter are evaluated. Additionally, samples with and without rapid thermal anneal (RTA) treatment are part of these experiments. The deposition process from 850 °C up to 1150 °C is based on previous work [3]. Additional experiments and measurements presented in this publication examine the crystallographic properties by electron backscatter diffraction (EBSD) and Raman spectroscopy. The electrical quality of the µc-Si layers is investigated by light beam induced current (LBIC) and complemented by the transfer length method (TLM) and SunsVoc measurements.

Keywords: a-Si/µ-Si, Micro Crystalline Si, Si-Films, Thin Film Solar Cell, Epitaxy, CVD Based Deposition

1 INTRODUCTION

Various companies and institutions are working on crystalline silicon thin-film (cSiTF) solar cells to reduce material and wafering costs. The CSG Solar AG presented a mini module on borosilicate glass using µc-Si layers with an efficiency of 10.4 % [1] and Oerlikon presented their micromorph tandem with a columnar structure. The microcrystalline structure changes depending on the deposition temperature and the layer thickness. Electron backscatter diffraction measurements show grain sizes of 0.5-10.0 μm with a columnar structure. The doping concentration depending on cell concept and layer thickness. The diffusion process from 850 °C up to 1150 °C has been simulated and optimised for two different solar cell concepts featuring different metallisation schemes and a comparison between epitaxial µc-Si emitter, diffused POCl3 emitter, and plasma enhanced chemical vapour deposition (PECVD) deposited a-Si heterojunction solar cells.

Figure 1: Solar cell concepts (not in scale) with µc-Si layers deposited by APCVD on conductive substrates with front and backside metallisation (top) and with single-side contacts on nonconductive substrates (bottom).

2 EXPERIMENTAL PROCEDURE

APCVD offers a fast, high throughput and cost effective alternative for the deposition of µc-Si films on various substrates. This presented laboratory approach is also transferable to the industrial production-type (ProConCVD) reactor with a capacity of ~30 m²/h [4].

2.1 Deposition of µc-Si layers by APCVD

The µc-Si depositions presented in this paper have been done in two different APCVD reactors. Based on the deposition and characterisation of µc-Si layers processed at 850 °C up to 1000 °C on a small scale laboratory reactor at ISE [3], a deposition process for n- and p-type µc-Si films...
The deposition thickness of an average μc-Si layer deposited at the RTCVD160 reactor using standard conditions.

using a quasi-inline reactor has been optimised. In the case of the RTCVD160 reactor, samples with a size up to 100x100 mm² are placed in a parallel reactor. The deposition is done using trichlorosilane (TCS) as precursor and phosphine (PH₃) and diborane (B₂H₆) as dopant source. Depositions with different process parameters (850-1150 °C; 2.5-5.5 g/min SiHCl₃ in H₂) on various intermediate layers, for instance SiNₓ, SiOₓ, and SiCₓ, have been done. Through adjustments of the deposition process and the sample placement it was possible to improve the layer thickness homogeneity (see Fig. 2) and to get a better understanding of the μc-Si growth by APCVD. However, the homogeneity is still limited due to boundary effects and temperature gradients of the laboratory scale reactor.

The different μc-Si films where deposited on SiNx or SiOx layers. The standard deposition rate of 0.95 μm/min at 900 °C can be varied by changing the Cl/H ratio and the deposition temperature (see Fig. 3) and is dominated by the formation of dichloro-silane (H₂SiCl₂) in the gas flow [5]. Naturally by changing these parameters the p- and n-type layer doping by boron (1 x 10¹⁵ cm⁻³ to 1 x 10²⁰ cm⁻³) and phosphorous (1 x 10¹⁷ cm⁻³ to 1 x 10²⁰ cm⁻³) is changing and has to be analysed and adjusted. Since electrochemical capacitance voltage (ECV) measurements are not very reliable because of the μc nature of the layers, spreading resistance profiling (SRP) measurements of differently doped layers deposited at temperatures from 850 °C up to 1150 °C have been analysed.

2.2 Solar cell structure, processing and metallisation

The two solar cell concepts shown in Fig. 1 have been simulated to determine the back surface field (BSF) and absorber layer thickness [3]. Based on the results the depositions for two solar cell batches have been done. The SiOₓ layer of about 105 nm acts as an antireflection and passivation layer. The solar cell structure features an approx. 2 μm thick BSF and a 10 μm absorber. The BSF is relatively thick because it acts not only as field effect passivation but also as a buffer layer because the first 2 μm of directly deposited μc-Si show very high levels of stress and small grain sizes. Additional simulations of an optimised BSF and experiments investigating the nucleation of μc-Si on SiNx and SiOx are ongoing. Depending on the batch, a 750 nm μc-Si emitter is deposited in-situ. The second concept, including a front and back contact formation is connected with the conductive substrates by laser fired access (LFA) after the BSF deposition (see Fig. 4). The pitch has been optimised using Pitchmaster Version 2.1, a simulation tool developed by ISE. Furthermore, experiments to test the etching of the mesa structures using 8% KOH at 85 °C with 0.9±0.1 μm/min, 40% KOH at 85 °C with 0.8±0.1 μm/min and plasma etching with 1.7±0.1 μm/min have been done. Samples for additional measurements like transfer length method (TLM) and SunsVoc have also been prepared.

Deposition and sample preparation for crystallographic and electrical characterisation

In addition to the solar cell batch two different batches for characterisation have been processed. The first batch for EBSD measurements features 8 μm and 30 μm thick μc-Si layers on BSG glass and Si substrates both with SiNx and SiOx as intermediate layers. These EBSD measurements have been done in collaboration with HZB Berlin. The samples have been polished with a 100 nm diamond-lapping film and ion milling. Afterwards a graphite layer of a few nm thickness has been deposited. This extensive preparation is necessary to achieve high signal intensities for fitting the Kikuchi pattern. The second batch is a continuation of the Raman experiments presented in a previous paper [3]. The samples have been deposited at different temperatures and with different thicknesses. Subsequently, a number of samples received a rapid thermal anneal (RTA) or a zone melting recrystallisation
(ZMR) as post treatment. Further sample information is listed below in Table I. The detailed sample preparation can differ because these samples were used for surface measurements and cross sections as well. Furthermore these samples were also used for conductive atomic force microscopy (C-AFM) measurements.

**Table I:** Deposition temperature and post treatment.

<table>
<thead>
<tr>
<th>Sample no.</th>
<th>Layer</th>
<th>Temperature [°C]</th>
<th>Post treatment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>µc-Si 10 µm</td>
<td>1100</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>µc-Si 15 µm</td>
<td>1000</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>µc-Si 20 µm</td>
<td>950</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>µc-Si 10 µm</td>
<td>850</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>µc-Si 30 µm</td>
<td>850</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>µc-Si 10 µm</td>
<td>1100</td>
<td>RTA</td>
</tr>
<tr>
<td>7</td>
<td>µc-Si 15 µm</td>
<td>1000</td>
<td>RTA</td>
</tr>
<tr>
<td>8</td>
<td>µc-Si 20 µm</td>
<td>950</td>
<td>RTA</td>
</tr>
<tr>
<td>9</td>
<td>µc-Si 10 µm</td>
<td>850</td>
<td>ZMR</td>
</tr>
<tr>
<td>10</td>
<td>µc-Si 30 µm</td>
<td>850</td>
<td>ZMR</td>
</tr>
</tbody>
</table>

3 RESULTS AND DISCUSSION

3.1 Crystallographic characterisation

3.1.1 Electron backscatter diffraction

The characterisation by EBSD enables us to determine grain orientation, grain size and grain distribution. Sample surfaces and cross sections have been used to determine not only the horizontal (parallel to the substrate) but also the vertical (perpendicular to the substrate) grain size. The quality of cross section EBSD measurements is limited due to a low signal-to-noise ratio for cross sections. Consequently, unclear maxima after the Hough-Transformation cause weak Kikuchi patterns and ultimately appear like grain boundaries or possibly false nano-crystalline clusters (see Fig.5 red circle). The EBSD maps in Fig. 5 shows grain sizes of about 0.5-10 µm depending on the layer thickness. The first 2 µm of the layer consists of very small grains due to the random nucleation on the intermediate layers.

![Figure 5: EBSD cross section measurements of µc-Si layers grown on BSG (left) and on monocrystalline silicon with intermediate layer (right). The substrates are in both cases on the left side.](Image)

The columnar growth and the dominant epitaxial growth of preferential grain orientations influences the growth of µc-Si layers by APCVD and grains of 5-10 µm and can be seen on both substrates. These results can be compared to the µc-Si layers by SPC with an average grain size of 1-2 µm [6], aluminium induced crystallisation (AIC) with a grain size of 5-20 µm [7] and electron beam crystallisation (EBC) with grain lengths of several 100 µm but with a large number of small angle grain boundaries/twins [8]. However, the EBSD measurements show one of the main advantages of APCVD compared to EBC and AIC. As a result of the columnar growth by APCVD deposition the µc-Si layers have a large vertical grain size and therefore relatively a higher diffusion length as described in [9].

3.1.2 Raman spectroscopy

Generally, the analysis of Raman spectra can be used to investigate the grain size, grain distribution, Shockley-Read-Hall (SRH) lifetime, stress and defect density. In this case µc-Si layers on Si substrates and BSG substrates with SiN₄ will be examined. The majority of the samples have been characterised on an optimised µRaman setup at the FZU in Prague. The spectra are measured by using a 100x objective, 1 s accumulation time, a laser intensity of ~10 mW on the sample and a laser spot of ~ 400 nm.

![Figure 6: Raman spectra of a µc-Si layer with a thickness of 10 µm on a Si substrate with SiN₄](Image)

The typical c-Si Raman spectra consists of a narrow (approx. 5 cm⁻¹) band at 520.5 cm⁻¹. The spectra of µc-Si layers in Fig. 6 show an additional band around 495 cm⁻¹. This band at 495 cm⁻¹ is usually interpreted as a wurtzite c-Si structure [10, 11]. In our case its intensity is always well correlated with the width of the LO-TO band and therefore with defects in the layer (see Fig. 7).

![Figure 7: Analysis of a) 3rd band intensity, b) width of c-Si band, c) c-Si band intensity and d) c-Si band shift of a 30 µm thick µc-Si layer on SiN₄](Image)
Areas with a similar defect density are elongated in the vertical growth direction. The stress in the layer can be determined by the shift of the c-Si band (see Fig. 7) which is not directly correlated with defects in the layer. Similar in all Raman measurements is the transition from compressive stress (bright area in the Raman shift analysis in Fig.7) close to the interface into tensile stress (dark areas) towards the surface of the layer.

The Lorentz fit of the peak centre (487-505 cm\(^{-1}\)) reveals regions with defects, dislocations and grain boundaries as discussed above. Therefore it is apparent that the first ~2 µm of the layer are areas with high defect densities. This agrees with EBSD measurements, showing the nanocrystalline Si structure close to the intermediate layers due to the random nucleation [12]. Consequently, depending on the layer thickness only larger grains remain due to columnar growth and preferential orientations. The correlation between defect density and the 3\(^{rd}\) band area has also been used to investigate the influence of the deposition temperature, RTA or ZMR treatment on stress and defect density. The samples used in this batch are listed in Table I. In Fig. 8 the relative peak intensity between the 495 cm\(^{-1}\) and 520.5 cm\(^{-1}\) peak (bottom) as well as the peak width of the 520.5 cm\(^{-1}\) band (top) are shown for all samples. The deposition at 850 °C shows the highest defect density, whereas the deposition at 1100 °C shows the lowest. A close analysis of the deposition at 1100°C also reveals a difference in the peak width of the 520.5 cm\(^{-1}\) band and the relative peak intensity for defect analysis. The relative peak intensity is zero (there is no 495 cm\(^{-1}\) band) for depositions at 1100°C, which is similar to the c-Si without defects. Since the peak width for these samples is well above 5 cm\(^{-1}\) the peak width analysis apparently includes types of defects which are not included in the analysis of the relative peak intensity. This effect could be used to distinguish between different types of defects [13], which are more sensitive to annealing. The samples that have been processed by ZMR support these findings because there is no Raman band at 495 cm\(^{-1}\) and therefore only the “standard” defect centre visible in the Raman spectra. The RTA treatment is most effective for depositions between 850 °C up to 950 °C and shows almost a reverse effect for depositions at 1100 °C because no annealing sensitive defects are present in these layers. Obviously, the additional annealing allows impurities to diffuse from the grain boundaries into the grain.

The stress distribution in these layers (see Fig. 9) shows a similar pattern compared to the defect results. The stress in the as-deposited layer (shift from the 520.5 cm\(^{-1}\) to the free c-Si position) is decreasing with increasing temperature. After the annealing step, the stress is negligible (bellow the resolution of Raman experiment).

**Figure 8:** Raman spectra band width (top) and relative peak intensity at the 495 cm\(^{-1}\) band (bottom) for different deposition parameters and post deposition treatments.

**Figure 9:** The shift of the Raman spectra represents the stress inside of the µc-Si layers and distinguishes between tensile and compressive stress.

### 3.2 Solar cell results

Different polycrystalline and µc-Si layers by SPC and electron beam crystallisation have already been simulated [14, 15]. Based on these publications and previous experiments, simulations of the cell concept with µc-Si layers on conductive substrates with front and backside metallisation using PC1D have been done [3]. According to these simulations two different solar cell batches have been processed. The basic concept of the first batch is shown in Fig. 1 (bottom) which has been done in cooperation with IMEC. The goal of the first batch is a comparison of a µc-Si emitter, which can be deposited in-situ, and an a-Si emitter. The single-side contact scheme, for comparison in both cases, has been adjusted to contact an a-Si emitter. The results (see Table II) show that voltages up to 466 mV have been reached using a 10 µm µc-Si/a-Si layer stack. However, due to the lack of light trapping and proper texturing a current of only 9 mA using a 10 µm µc-Si absorber in combination with a µc-Si emitter has been
achieved. The energy conversion efficiency is also limited by the fill factor of 60% and reaches a maximum of only 2.8%. A comparison with and without RTA has only been done with the μc-Si/a-Si solar cells. In agreement with the Raman analysis (deposited at 950 °C) the RTA treatment features an increase in voltage of 16 mV.

Table II: IV-Characteristics of solar cells comparing μc-Si layers with μc-Si emitter and a-Si emitter in a concept featuring a single side contact scheme.

<table>
<thead>
<tr>
<th>Concept</th>
<th>V_{OC} [mV]</th>
<th>J_{SC} [mA]</th>
<th>FF [%]</th>
<th>n [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>μc-Si/a-Si (1)</td>
<td>466</td>
<td>8.4</td>
<td>69</td>
<td>2.7</td>
</tr>
<tr>
<td>μc-Si/a-Si (2)</td>
<td>429±31</td>
<td>8.5±0.3</td>
<td>58±7</td>
<td>2.1±0.4</td>
</tr>
<tr>
<td>μc-Si/a-Si + RTA (1)</td>
<td>457</td>
<td>8.8</td>
<td>68.7</td>
<td>2.8</td>
</tr>
<tr>
<td>μc-Si/a-Si + RTA (2)</td>
<td>445±16</td>
<td>8.5±0.5</td>
<td>62±7</td>
<td>2.4±0.4</td>
</tr>
<tr>
<td>μc-Si/μc-Si + RTA (1)</td>
<td>408</td>
<td>9.0</td>
<td>7.0</td>
<td>2.6</td>
</tr>
<tr>
<td>μc-Si/μc-Si + RTA (2)</td>
<td>399±31</td>
<td>8.5±0.3</td>
<td>58±7</td>
<td>2.1±0.4</td>
</tr>
</tbody>
</table>

(1) – Best cell; (2) – Average out of at least 6 cells

The concept of the second batch is shown in Fig. 1 (top). In this case a diffused POCl₃ emitter has been used in combination with a 10 µm absorber deposited at 950°C. The voltages of 226 mV without and 274 mV with RTA are significantly lower compared to the first batch. This can partially be explained by the passivation quality of a-Si emitters, but compared to the μc-Si emitter it is still a significant loss in voltage. However, the current of 14.7 mA is a reasonable result for a 10 µm absorber without light trapping and texturing. Although similar μc-Si absorber layers have been used in both cases, the different cell concepts show different result. The critical process steps like passivation, hydrogenation, mesa structuring, and contact formation have to be further investigated and optimised.

Table III: IV-Characteristics of a solar cell batch using a diffused POCl₃ emitter.

<table>
<thead>
<tr>
<th>Concept</th>
<th>V_{OC} [mV]</th>
<th>J_{SC} [mA]</th>
<th>FF [%]</th>
<th>n [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>POCl₃</td>
<td>226±2</td>
<td>14.7±0.4</td>
<td>50±1</td>
<td>1.7±0.1</td>
</tr>
<tr>
<td>POCl₃ + RTA</td>
<td>274±7</td>
<td>14.2±0.2</td>
<td>56±0</td>
<td>2.2±0.1</td>
</tr>
</tbody>
</table>

Averages out of only 2 cells

3.3 Solar cell characterisation

The solar cells with μc-Si layers cannot be improved by crystallographic characterisation alone but also by optimising the presented cell concepts. Therefore standard IV-curve measurements, TLM measurements, SunsVoc measurements, and LBIC measurements have been done for solar cell characterisation methods.

3.3.1 Spectral response measurements

In Fig. 10 the IQE, EQE, and Reflection of a solar cell with front and backside metallisation (second batch) with diffused POCl₃ emitter is shown. The reflection of approx. 9% is typical for cSiTF solar cells on silicon substrates with intermediate layer. The steep decrease of IQE and EQE values above 550 nm is expected for μc-Si material featuring lifetimes below 1 μs. The low IQE and EQE from 400 nm up to 500 nm show that the emitter is limited by high defect densities. The reflection is influenced by the antireflection coating, a rough surface, and poor light trapping inside the active layer.

3.3.2 Transfer length method (TLM) measurements

TLM measurements have been done on simplified test structures and on finished solar cells that have been cut into stripes. In Fig. 11 (left) a TLM structure realised by evaporating aluminium contacts on different μc-Si layers is shown.

Figure 10: EQE, IQE, and reflection of a solar cell with front and backside metallisation (second batch) with diffused POCl₃ emitter.

Figure 11: Simplified TLM structures (25x25 mm²) realised by evaporating aluminium contacts on different μc-Si layers (left) and fitting of the contact resistance (right).

The determination of the contact resistance (ρc below ~6 mΩcm² has no significant influence on series resistance (16), series resistance, and the transfer length L_T can be used to evaluate material properties and to adjust the cell concept as well as grid metallisation. These measurements are also necessary to improve solar cell simulation. The detailed measurement results of a POCl₃ emitter on μc-Si with ρc ~3.4 mΩcm² and of a μc-Si emitter with ρc ~7.3 mΩcm² are shown in Table IV. The determination of R_s by fitting the dark IV-curves has not been possible because reliable fitting parameters could not be determined. Therefore, SunsVoc measurements have been correlated with illuminated IV-curves to determine a R_s of 0.83 Ωcm² (R_s of 0.6 Ωcm² is only a 2 mV loss in voltage at 0.9 suns [16]). However, the TLM measurements show that the front contact formation itself is no limiting factor for concepts featuring μc-Si emitters.

Table IV: TLM results of finished solar cells with evaporated TiPdAg seed layer and plated Ag.

<table>
<thead>
<tr>
<th>Emitter type</th>
<th>ρc [mΩcm²]</th>
<th>R_s [Ω]</th>
<th>R_b [Ω/sq.]</th>
<th>L_T [μm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>POCl₃</td>
<td>3.4</td>
<td>2.0</td>
<td>53</td>
<td>35</td>
</tr>
<tr>
<td>μc-Si</td>
<td>7.3</td>
<td>2.1</td>
<td>81</td>
<td>129</td>
</tr>
</tbody>
</table>
3.3.3 Light beam induced current (LBIC) measurements

Passivation and minority carrier lifetime, respectively the diffusion length of µc-Si layers are obviously critical factors. Preliminary measurements with an updated MWPCD (microwave photo conductance decay) at the Fraunhofer ISE show effective minority carrier lifetimes of 250-500 ns. These measurements show a high systematic error because of a low signal to noise ratio despite using a green excitation laser for cSiTF and an upgraded microwave detector [17]. It is also difficult to calculate the diffusion length (\( L_d \)) using these results because the carrier mobility of µc-Si is still under investigation [18, 19].

Processing solar cells has the advantage that the diffusion length can be determined by light beam induced current (LBIC) measurements (see Fig. 12). The measurement tool (LOANA by pv-tools) used for these measurements includes four excitation wavelengths of 532 nm (\( \alpha^1 \sim 1.3 \) µm), 670 nm (\( \alpha^1 \sim 4.2 \) µm) and 780 nm (\( \alpha^1 \sim 9.9 \) µm) which are relevant for an absorber layer of only 10 µm. These measurements show a diffusion length of only ~7.5-20 µm. Assuming a diffusion of coefficient \( D_a \sim 18.5 \) cm²/s and mobility of \( \mu_a \sim 716.3 \) cm²/Vs for c-Si (\( \rho \sim 0.25 \) Ω cm) a lifetime of 150 ns has been determined which is below our MWPCD measurements.

\[ L_{\text{eff}} = 17.7 \text{[m]} \]

Figure 12: Diffusion length determination by fitting the inverse IQE for 532 nm and 670 nm of cSiTF solar cells with µc-Si layers by APCVD.

\[ L_{\text{eff}} \text{[m]} \]
- 30.0
- 27.5
- 25.0
- 22.5
- 20.0
- 17.5
- 15.0
- 12.5
- 10.0
- 7.5
- 5.0

Figure 13: Mapping of the effective diffusion length by measuring the quantum efficiency at 532 nm and 670 nm.

4 CONCLUSION

This paper investigates and examines the deposition of µc-Si films with grain sizes of 0.5-10 µm by APCVD and their integration into two different solar cell concepts. The depositions have been made at temperatures between 850 °C up to 1150 °C and deposition rates of ~1.6 µm/min have been achieved.

The presented experiments evaluate the crystallographic and electronic quality of the µc-Si films (\( V_{OC} \) of 466 mV) including the parameters \( \rho_s, L_e, V_{eff}, R_s \). The solar cell results show a current of ~14 mA without light trapping and texturing for a 10 µm thick absorber. Different deposition temperatures and post-treatments like ZMR and RTA (improvement of ~20 mV respectively 50 mV), which are necessary to increase the overall material quality, have been analysed by Raman spectroscopy. A differentiation between defects which are more sensitive to annealing and the qualitative determination of stress inside the µc-Si layers has also been done by Raman spectroscopy. The specific contact resistance of \( \rho_s \sim 5 \) mΩ/cm² and the series resistance of 0.83 Ωcm² show that the optimised contact and metallisation scheme are well suited for the µc-Si solar cell concepts presented in this paper. However, LBIC measurements indicate low lifetimes of ~150 ns for µc-Si layers. These results lead to the conclusion that the absorber layer has to be reduced to a thickness of 6 µm.

A different application for the µc-Si layers is the recrystallisation of these layers. On glass using e-beam crystallisation voltages of 539 mV have been achieved. A more industrial feasible approach is the crystallisation by ZMR resulting in voltages of 614 mV [20].

5 ACKNOWLEDGEMENT

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